**An Efficient Design Of 16 Bit MAC Unit Using Vedic Mathematics**

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# Abstract:

Multiply and Accumulate (MAC) is one of the primary operations used widely in signal-processing and other applications. Multiplier is the fundamental component of Digital Signal Processors (DSP's).Its parameters such as power, LUT utilization and delay decides the performance of a DSP. So, there is a need to design a power and delay efficient multiplier. In this paper, a 16-bit MAC unit is designed using an 8-bit vedic multiplier and carry-save adder. A comparison with the existing 8-bit vedic multiplier using Square-Root (SQR) Carry-Select Adder (CSLA) is presented. It is compared with a conventional array-multiplier. The entire design is implemented in Verilog HDL.

**Tools used:**

**Xilinx 13.2**